W-Band InP Wideband MMIC LNA with 30K Noise Temperature

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ABSTRACT

This paper describe a millimeter wave low noise amplifier with extraordinary low noise, low power consumption, and wide frequency range. These results are achieved utilizing state-of-the-art InP HEMT transistors coupled with CPW circuit design. The paper describes the transistor model, modeled and measured on-wafer and in-module results at both 300K and 24K operating temperatures for many samples of the device.

INTRODUCTION

The applications for low-noise amplifiers above 75 GHz are compact surveillance radars including automotive radar, very wideband communications, measurements of the temperature and constituents of the atmosphere, and both ground-based and spaceborne radio astronomy. In the latter case cryogenically-cooled amplifiers are required to achieve the desired sensitivity and superconducting SIS mixers are a competitive technology. Previous papers have described GaAs and InP MMIC amplifiers operating at room temperature with noise temperatures in the 300 to 500K range [1]. A discrete InP transistor MIC LNA cooled to 20K with a noise temperature of 60K has been previously reported by Pospieszalski [2]. In this publication we will describe a cryogenically-cooled MMIC LNA which covers the 65 to 110 GHz with an average noise temperature of 45K and a minimum noise of 30K at 102 GHz measured at the waveguide flange. Results for 6 modules and measurements of the noise and gain as a function of the phase of generator reflection coefficient are reported In addition to this excellent noise performance, the device has a unique pilot-signal path for gain monitoring and can produce 20 dB gain with as little as 1.4 mW of DC power.

(Companion papers describing the CPW to waveguide transition used in the MMIC module [3] and a cryogenic radiometer system using 16 of the MMIC LNA's [4] have been submitted to the 1999 MTT-S.}

DESIGN AND FABRICATION (Summary)

The MMIC was designed for an advanced development 0.1uM InP transistor recently developed at TRW [5] The MMICAD circuit simulator was used with a transistor model determined by extensive "hot-fet, cold-fet" [6] measurements of sample transistors in a CPW test structure. The circuit was realized using CPW transmission lines along with thin film capacitors (0.3 fF/um^2) and thin file resistors (100 ohms/square). The layout of the circuit is shown in Figure 1, the transistor model used for the design is listed in Figure 2, and the waveguide module incorporating the MMIC device is shown in Figure 3. Note that the circuit model uses the Pospieszalski noise model [7] with ambient temperature , Tamb, noise assigned to all resistors except Rds which is assigned a drain noise temperature value, Td of 300K + 6* Tamb. This noise model gives good correlation with the measured results.

An unusual feature of the circuit design is a VHF pilot-signal path through the same transistors used for the millimeter wave signal. The pilot signal, typically 500 MHz, is applied through a pilot input terminal (upper left pad in Figure 1) and appears at a pilot output pad (upper right). The low-level pilot signal is coupled from one bias circuit to the next with no interaction with the millimeter-wave signal. The purpose is to measure gain fluctuations of the transistors in applications such as radiometry which are sensitive to these fluctuation. Results of applying this technique to a GaAs MMIC are described in [8] where an improvement in gain stability of 2.7 was achieved. The pilot signal stabilization has not been tested for the InP MMIC described in this present paper.

MEASURED RESULTS (Summary)

The gain and input return loss as measured with wafer probes (50 to 75 GHz and 80 to 115 GHz) is compared with the circuit model in Figure 4. The gain measured in the waveguide module is also shown. In general the agreement is excellent.

Seventeen modules were constructed and tested. The noise temperature was tested with a variable temperature waveguide 20 dB attenuator with temperature measured with a precision temperature sensor. The range of noise temperature over the 85 to 115 GHz range for all modules was 30 to 107K at an operating temperature of 24K; the noise of the best 6 modules is plotted in Figure 5. Noise at room temperature was in the range of 250K to 470K.

The DC bias (Vd, Id, Vg, and total DC power) was: at room temperature (1, 30, 0, 30 mW), at 24K for minimum noise (1, 10, 0, 10 mW) , at 24K for minimum DC power at 20 dB gain (0.25, 5.7, +.04, 1.4mW), and at 24K for minimum DC power at 15 dB gain (.15, 3.5, +.035, 0.53mW).

To assess whether the amplifier noise could be further reduce by revising the input network, a Teflon slug with length $\lambda/4$ was inserted approximately 2 cm from the MMIC input pads. This produces a generator refllection coefficient with magnitude 0.35 and phase which varies rapidly with frequency. The result shown in Figure 6 shows that the gain variation is in anti-phase with the noise temperature variation indicating that the generator impedances for gain match and noise match are very close; this is expected at cryogenic temperatures since most of the noise i is introduced in the output circuit of the transistor. The minima of the noise curves falling below the noise measured with matched waveguide, indicates that further improvement in the noise temperature is possible.

REFERENCES

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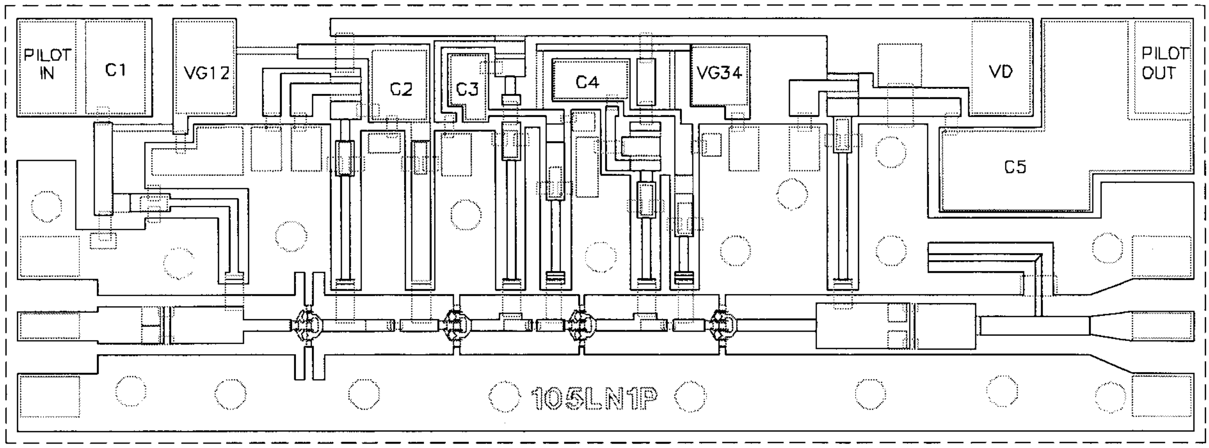

Figure 1 – MMIC layout. The chip size is 2 x 0.73 x .075 mm.

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! DEFINE  40*M um InP HEMT N60B Best  estimate
11/18/98
! From  UMass Data
! REF PLANES +/- 30 um FROM CENTER
! BIASED FOR PEAK GM
 IND  11 1   L=5 ! LG
 CAP  1 0  C=-10 !CPG
 RES  1 2  R={4/M} ! RG
 CAP  2 3  C={33*M} ! CGS
 RES  3 4  R=3 ! RI
 RES  4 10  R={8.2/M} ! RS
 IND   10  0 L=10 ! LS
 CAP  2 5  C={4.5*M} ! CFI
 CAP  5 4  C=-2 ! CDS -2
 RES  5 6  R=8.8 ! RD
 CAP  1 6  C=3 ! CFO
 CAP  6 0  C=19 ! CPD 10.5
 IND  6 7  L=0 ! LD
 VDCS  2 5 3 4  GM={61*M}  A=0 R1=1E6   R2=1E6
F=1E6 TAU=-0.5
 REST 5 4 R={168/M} T={300 + 6*TEMP}
 DEF2P 11  7     PHEMT
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Figure 2 – Circuit model of the InP HEMT device used in the MMIC design

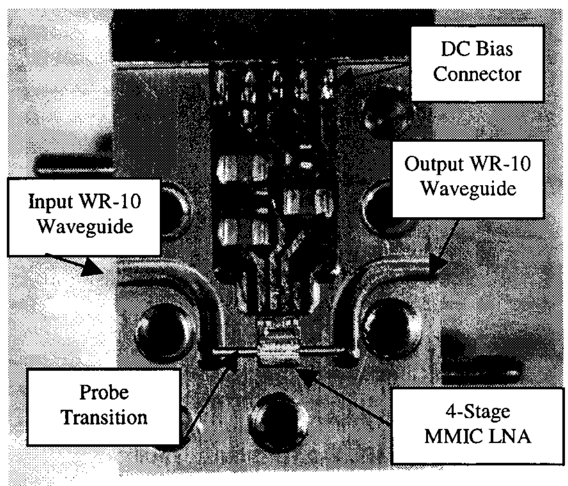

Figure 3 – Interior view of split-block module for MMIC device

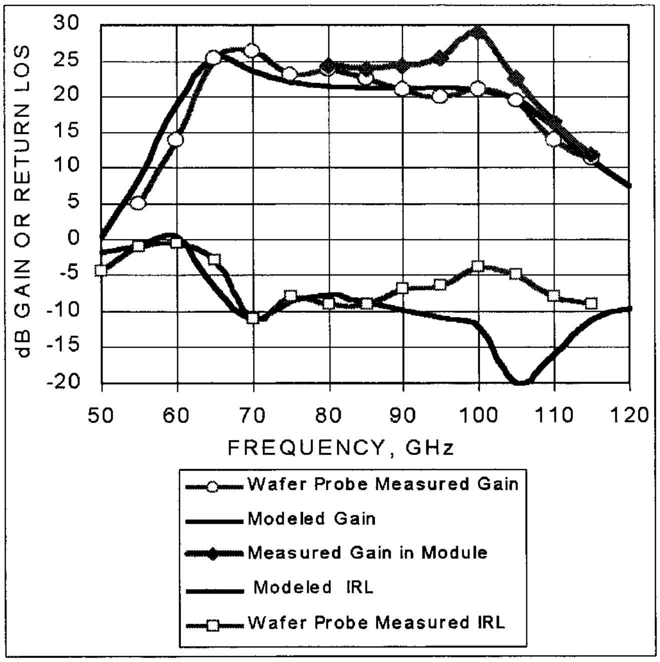

Figure 4 – Gain and input return loss, modeled and measured with wafer probes, and gain measured in waveguide module, all at 295K.

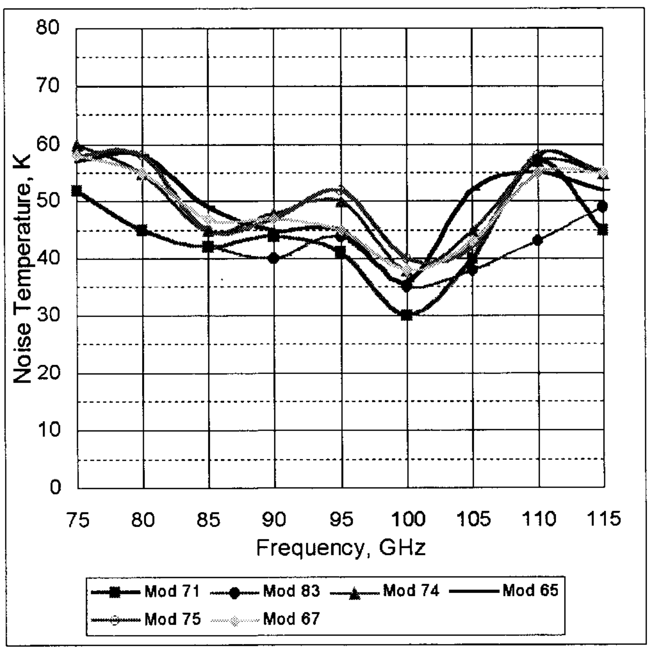

Figure 5 – Noise temperature of six waveguide modules at a temperature of 24K. The typical gain is shown in Figure 6 and typical bias is Vd=0.95V, Id=10 mA(total for all 4 stages), and Vg =0 +/- 0.1V.

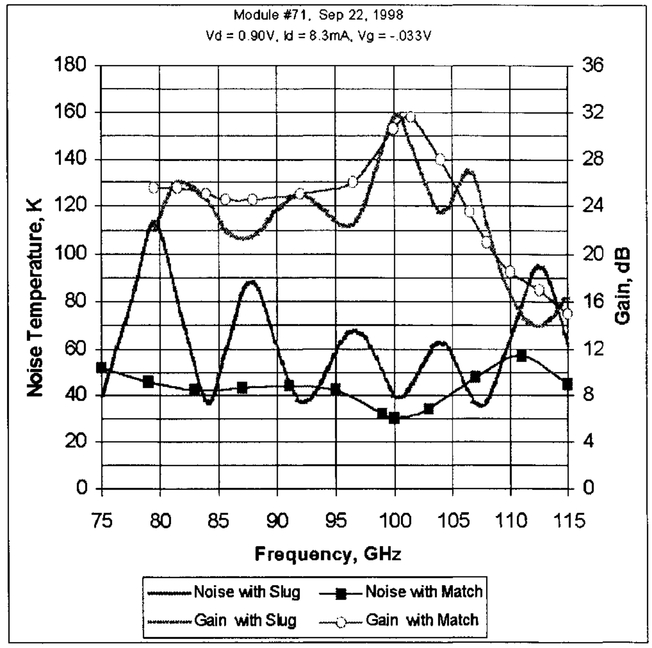

Figure 6 – Gain and noise temperature with matched source and with quarter-wave Teflon slug discontinuity in input waveguide to reveal gain and noise at a function of phase of generator reflection coefficient.